[ABSTRACT]

To provide a high-performance semiconductor integrated circuit in which the standby current is reduced by preventing current leakage in a semiconductor integrated circuit device, for example, the memory cell of an SRAM.

Gate electrode G is formed on semiconductor substrate 1 and n^+-type semiconductor regions 17 (source/drain regions) are formed in the semiconductor substrate on both sides of this gate electrode. Within the same apparatus and under near-vacuum conditions, a depth of 2.5 nm or less is etched away from the surfaces of the source/drain regions and gate electrode, a film of Co is then formed on the source/drain regions, and thermal processing is applied to form $CoSi_2$ layer 19a. As a result, current leakage in the memory cell can be prevented and this method can be applied to semiconductor integrated circuit devices that have low current consumption or are battery-driven.